What is claimed is:

1. A system for serial data communication between a first IC chip and a second IC chip, the first IC chip having a first data transmitter and a first data receiver, the second IC chip having a second data transmitter and a second data receiver, the system operating in response to a synchronization clock signal, the system comprising:

a transfer request signal generator, for generating a transfer request signal;

a control signal generator, for generating a transfer control signal in response to the transfer request signal, the transfer control signal having a first state for indicating the data communication being active and a second state for indicating none of the data communication being active; and

an input/output control signal generator, for generating an input/output control signal in response to the synchronization clock signal when the transfer control signal is in the first state, wherein the data communication between a first IC chip and a second IC chip is controlled by the input/output control signal.

2. The system of claim 1, wherein a time period of the first state of the transfer control signal has a plurality of intervals, if data is transmitted from the first IC chip to the second IC chip, the first data transmitter of the first IC chip transmitting the data during one of the intervals in the first state and the second data receiver of the second IC chip receiving the data during the same interval.

3. The system of claim 2, wherein the synchronization clock signal has a plurality of cycle periods, each of the intervals of the first state of the transfer control signal is synchronized by the corresponding cycle period of the synchronization clock signal.

4. The system of claim 1, wherein a time period of the first state of the transfer

control signal has a plurality of intervals, if one of data bits is transmitted from the first IC chip to the second IC chip, the first data transmitter of the first IC chip transmitting the data bit during one of the intervals in the first state and the second data receiver of the second IC chip receiving the data bit during the same interval.

5. The system of claim 4, wherein the synchronization clock signal has a plurality of cycle periods, each of the intervals of the first state of the transfer control signal is synchronized by the corresponding cycle period of the synchronization clock signal.

6. The system of claim 1, wherein a time period of the first state of the transfer control signal has a plurality of intervals, if a plurality of data bits are transmitted from the first IC chip to the second IC chip, the first data transmitter of the first IC chip transmitting the data bits during one of the intervals in the first state and the second data receiver of the second IC chip receiving the data bits during the same interval.

7. The system of claim 6, wherein the synchronization clock signal has a plurality of cycle periods, each of the intervals of the first state of the transfer control signal is synchronized by the corresponding cycle period of the synchronization clock signal.

8. The system of claim 1, wherein a time period of the first state of the transfer control signal has a plurality of intervals, if a first data bit is transmitted from the first IC chip to the second IC chip and a second data bit is transmitted from the second IC chip to the first IC chip,

the first data transmitter of the first IC chip transmitting the first data bit during a first one of the intervals in the first state and the second data receiver of the second IC

chip receiving the first data bit during the same interval,

the second data transmitter of the second IC chip transmitting the second data bit during a second one of the intervals in the first state and the first data receiver of the first IC chip receiving the second data bit during the same interval.

9. The system of claim 8, wherein the synchronization clock signal has a plurality of cycle periods, each of the intervals of the first state of the transfer control signal is synchronized by the corresponding cycle period of the synchronization clock signal.

10. The system of claim 1, wherein a time period of the first state of the transfer control signal has a plurality of intervals, if a plurality of first data bits are transmitted from the first IC chip to the second IC chip and a plurality of second data bits are transmitted from the second IC chip to the first IC chip,

the first data transmitter of the first IC chip transmitting the first data bits during a first one of the intervals in the first state and the second data receiver of the second IC chip receiving the first data bits during the same interval,

the second data transmitter of the second IC chip transmitting the second data bits during a second one of the intervals in the first state and the first data receiver of the first IC chip receiving the second data bits during the same interval.

11. The system of claim 10, wherein the synchronization clock signal has a plurality of cycle periods, each of the intervals of the first state of the transfer control signal is synchronized by the corresponding cycle period of the synchronization clock signal.

12. A system for serial data communication between a first IC chip and a second

IC chip, the first IC chip having a first data transmitter and a first data receiver, the second IC chip having a second data transmitter and a second data receiver, the system operating in response to a synchronization clock signal, the system comprising:

a transfer request signal generator, for generating a transfer request signal;

a control signal generator, for generating a transfer control signal in response to the transfer request signal, the transfer control signal having a first state for indicating the data communication being active and a second state for indicating none of the data communication being active, wherein a time period of the first state of the transfer control signal has a plurality of intervals; and

an input/output control signal generator, for generating an input/output control signal in response to the synchronization clock signal when the transfer control signal is in the first state, wherein

if a plurality of data bits are transmitted between the first IC chip and the second IC chip, a portion of the data bits being transmitted from the first IC chip to the second IC chip during a first interval of the intervals and other portions of the data bits being transmitted from the second IC chip to the first IC chip during a second interval of the intervals.

13. The system of claim 12, wherein the synchronization clock signal has a plurality of cycle periods, each of the intervals of the first state of the transfer control signal is synchronized by the corresponding cycle period of the synchronization clock signal.

14. A method for serial data communication between a first IC chip and a second IC chip, comprising:

generating a transfer request signal;

generating a transfer control signal in accordance with the transfer request

signal;

generating an input/output control signal in response to a synchronization clock signal when the transfer control signal is activated, wherein the synchronization clock signal has a plurality of cycle periods;

in response to the input/output control signal, transmitting one data bit of the data desired to communicate between the first IC chip and the second IC chip by one of the first IC chip and the second IC chip, and receiving the transmitted data bit by the other of the first IC chip and the second IC chip within the cycle period of the synchronization clock signal.

15. A method for serial data communication between a first IC chip and a second IC chip, comprising:

generating a transfer request signal;

generating a transfer control signal in accordance with the transfer request signal;

generating an input/output control signal in response to a synchronization clock signal when the transfer control signal is activated, wherein the synchronization clock signal has a plurality of cycle periods;

in response to the input/output control signal, transmitting a plurality of data bits of the data desired to communicate between the first IC chip and the second IC chip by one of the first IC chip and the second IC chip, and receiving the transmitted data bits by the other of the first IC chip and the second IC chip within the cycle period of the synchronization clock signal.